REMARKS

In an Office Action mailed July 9, 2004, claims 1-6 and 8-25 were pending and all claims were rejected. In response thereto Applicants are herein amending claims 1, 6, 8, 9, 15, 18, 21 and 25, canceling claim 14 and requesting the reconsideration and allowance of claims 1-6, 8-13 and 15-25. Applicants thank the Examiner for the thoroughness and quality of the past Office Actions.

Claim Rejections

Rejection of Claim 8 under 35 U.S.C 112, first paragraph

Claim 8 was rejected under 35 U.S.C. 112, first paragraph, as lacking enablement. The cause of the rejection was the incorrect recitation at line 7 of the past marked-up claim version of the element "second low-pass filter." The correct recitation is "sixth low-pass filter" and amendment of claim 8 is herein requested. Accordingly, withdrawal of the rejection of claim 8 is requested.

Rejection of Claim 1 under 35 U.S.C 112, second paragraph

Claim 1 was rejected as being indefinite in connection with the recital at line 3 of "said filter." Amendment of claim 1 is herein made to make clear that the recited filter is the recited "second low-pass filter." Accordingly, withdrawal of the rejection of claim 1 is requested.

Rejection of Claims 1-6, 8-13, 16-19 and 21-25 under 35 U.S.C 103(a)

Claims 1-6, 8-13, 16-19 and 21-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al. (U.S. Patent 5,442,709) in view of Reich (U.S. Patent 4,827,515) and Kawamura (U.S. Patent 5,202,925). In response, independent claims 1, 18, 21 and 25 are herein amended to particularly recite that a trigonometric function used to generate a signal containing a difference of left channel and right channel information is provided by using a digital phase lock loop after decimating a pilot signal component to a sampling rate to no more than substantially 12k samples per second. As explained in the specification at page 20, lines 9-19, the PLL permits phase estimation and correction in a cost effective manner because it may be operated at a very low sampling rate. The recited decimator reduces the sampling rate of the pilot signal to permit a cost effective PLL.

In a previous Office Action (paper number 5) mailed September 5, 2003, notice was taken in paragraph 4 at page 3 that Vogt et al. does not disclose a phase lock loop. Vogt et al. teaches a decoder having a circuit 21 that receives a pair of signals and produces signals proportional to the cosine and sine that doubles the phase of two sinusoidal error signals. In contrast, the recited decoder decimates a single pilot signal component to a significantly lower sampling rate, recited as not greater than substantially 12k samples per second, and uses a digital PLL to estimate the phase error. The low sampling rate permits the PLL to be accurate without complex circuitry as evidenced by the exemplary embodiment of FIG. 5.

Neither Vogt et al., Kawamura nor Reich illustrate or teach the use of a PLL to generate at least one trigonometric function as recited. As stated on pages 4 and 5 of the Office Action, Vogt et al. also do not disclose a number of the recited low

pass filters and decimators of the rejected claims. In forming the L-R signal, the Vogt et al. structure uses six multipliers. To form correction signals (CORR. SIGNALS) from the squaring circuitry 21 of FIG. 2 that are applied to the multipliers used to form the L-R signal, two signal paths SPC1 and SPC2, each using duplicative circuitry, are required. The recited claims simplify the structure, accuracy and cost by using a digital phase lock loop that uses only the pilot signal component.

Applicants acknowledge, as stated in the prior Office Actions, that it is known to simplify filter circuitry by performing prior decimation. Decimation circuits are also well known. It is also known to use high-cut circuits to remove high frequency noise components such as taught by Kawamura and acknowledged by Applicants in the specification at page 2, lines 14-16. Applicants further acknowledge that FIR filters are well known in this technology. By using a digital PLL operating at a low sampling rate on a single pilot signal component and efficiently forming L+R and L-R signals that are blended with efficient interference control, an improved cost effective decoder is provided. Applicants have reviewed the art made of record, but not relied upon, and respectfully submit that the rejected claims, as amended herein, are readily distinguishable, whether taken alone or in reasonable combination.

Rejection of Claims 14, 15, 19 and 20 under 35 U.S.C 103(a)

Claims 14, 15, 19 and 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al. (U.S. Patent 5,442,709) in view of Reich (U.S. Patent 4,827,515) and Kawamura (U.S. Patent 5,202,925) as applied to claims 1 and 18, and further in view of Patel et al. (U.S. Patent 5,479,449) and Whikehart et al. (U.S. Patent 5,936,438).

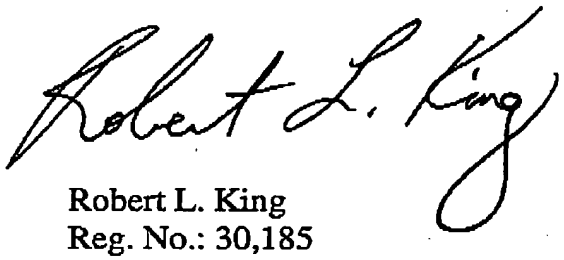
The addition of Patel and Whikehart to the basis of the rejection does not teach or suggest the claim recitals described above in connection with the amended base claims. Patel was cited for the proposition of teaching a phase-locked loop in the form of digitally controlled oscillator (270) and quadrature synchronous detector (250) of FIG. 5. The two circuits do not form a PLL. Instead, Patel discloses a digital oscillator that has a varying output between positive and negative representing digital descriptions of a carrier wave. Quadrature related phases are used to determine by using an adder when the carrier wave is positive or negative. The terms "PLL" and "phase-locked loop" do not exist in Patel. In contrast, the recited PLL of the rejected claims function to identify phase error associated with the (L-R) signal. There is no teaching or suggestion in Patel to use a PLL to generate at least one trigonometric function where the at least one trigonometric function represents "a phase angle needed to correct phase error associated with an output signal that contains a difference of left channel information and right channel information."

Whikehar et al. was cited for the proposition of using look-up tables to obtain sinusoidal signals. Applicants also acknowledge that this feature is notorious. However, as amended herein, claims 15, 19 and 20 and the underlying claims are readily distinguishable for the reasons provided above. Therefore, Applicants request the reconsideration and withdrawal of the rejection of claims 15, 19 and 20.

In view of the remarks set forth herein, claims 1-6, 8-13 and 15-25 of the application are believed to be in condition for allowance and a notice to that effect is solicited. No amendment made herein is related to the statutory requirements of patentability unless expressly stated herein. Further, no amendment herein is made for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular

reference or combination of references. In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,



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